REMARKS

Claims 1-25 are pending in the application. Claim 25 has been added by the present amendment. The amendment is fully supported by the specification as originally filed (see, e.g., page 34, line 23 to page 35, line 6).

With reference to claims 1 and 25, Applicants' claimed invention is directed to a shift register circuit having a plurality of register blocks, each register block having a flip-flop that operates in synchronization with a clock signal, and a transfer gate for controlling the clock signal supplied to the flip-flop. The transfer gate of a register block is brought into an ON-state **only** in a specified period during which an output of the flip-flop **changes** (claims 1 and 25).

With reference to FIG. 1, the transfer gate TG1 is brought into an ON-state only in a specified period during which the output OUT1 of the flip-flop FF1 changes (see, e.g., specification at page 35, lines 4-6). FIG. 2D represents a timing chart of the output OUT1, and FIG. 2C represents a timing chart of the control signal CTL1 for turning ON the transfer gate TG1. As shown in FIGS. 2C and 2D, the transfer gate TG1 is brought into an ON-state **only** when the output OUT1 of the flip-flop FF1 **changes**. As a result, consumption of power is reduced in the Applicants' claimed invention.

Claims 1-11 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,128,974 to Maekawa in view of U.S. Patent 5,602,561 to Kawaguchi et al. (hereinafter "Kawaguchi"). Claims 12-24 were rejected under 35 USC 103(a) as being unpatentable over Maekawa in view of Kawaguchi, and further in view of U.S. Patent 5,572,211 to Erhart et al. These rejections are respectfully traversed.

The Maekawa and Kawaguchi references, whether taken alone or in combination, fail to teach or suggest a shift register circuit in which a transfer gate is brought into an ON-state only in a specified period during which an output of the flip-flop changes.

With reference to FIG. 7 of Maekawa, as cited in the Office Action, the output from NOR gate NOR_1 is brought low when any one of the inputs to the NOR gate NOR_1 (i.e., $V_{(STRT)}$ and OUT_1) is brought high (see column 4, lines 49-52). When the output from the NOR gate NOR_1 is low, and the output VOR_1 of an inverter INV_4 is high, transfer gates SW_1 and SW_2 are brought into an ON-state (see column 4, lines 52-55). With reference to the timing charts of FIG. 8, the output VOR_1 of the inverter INV_4 is high when at least one of the input $V_{(STRT)}$ and the output OUT_1 of the unit register SR_1 is high (see column 4, lines 56-60). As shown in FIG. 8, the output VOR_1 of the inverter INV_4 has a period T of high level which is longer than that of the output OUT_1.

Therefore, Maekawa fails to teach or suggest that the transfer gates SW_1 and SW_2 are brought into an ON-state **only** in a specified period during which the output OUT_1 of the unit register SR_1 changes. In Maekawa, the transfer gates SW_1 and SW_2 are turned ON (indicated by the period T of the output VOR_1) for **longer** than a period of the output OUT_1 of the unit register SR_1.

In contrast, according to the Applicants' claimed invention, the transfer gate of a register block is brought into an ON-state only in a specified period during which an output of the flip-flop changes. For example, as shown in the timing diagrams of FIGS. 2C and 2D, the transfer gate TG1 (indicated by control signal CTL1) is brought into an ON-state **only** when the output OUT1 of the flip-flop FF1 **changes**.

Therefore, Maekawa fails to teach or suggest the Applicants' claimed invention as recited in claims 1 and 25. The Kawaguchi reference was cited merely for teaching D-type flip-flops connected in series, and thus fails to remedy the deficiencies of Maekawa.

With reference to claim 2, in Maekawa, when at least one of the input $V_{(STRT)}$ and output OUT_1 of the unit register SR_1 is high, then transfer gates SW_1 and SW_2 are brought into an ON-state (represented by the output VOR_1 of the inverter INV_4), as shown in FIGS. 7 and 8. In other words, the transfer gates SW_1 and SW_2 are turned ON by a combination of a high $V_{(STRT)}$ and

high OUT1, **or** by high and low signals. However, claim 2 requires that the level of an input signal inputted to each register block and the level of an output signal from the register block must **differ** from each other. In other words, according to the Applicants' claimed invention, the transfer gate of the register block is not brought into an ON-state when both the input and output signals are at a high level. Therefore, Maekawa fails to teach or suggest claim 2 of the Applicants' claimed invention.

Claims 3-24 incorporate the subject matter of claim 1, and thus are patentable over the cited combination of references, for at least the reasons discussed above.

It is believed that the claims are in condition for immediate allowance, which action is earnestly solicited.

Applicants believe that additional fees are not required for consideration of the within response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
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Date: December 30, 2003

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